In the Specification

Please replace the third paragraph on page 1, lines 22-26 with the following amended paragraph:

--In ~~a~~ patent application serial No. 08/968,598 filed on November 13, 1997 ~~even day herewith~~ under attorney docket number S1022/7945, now U.S. Patent No. 5,953,600 and incorporated herein by reference, a method for fabricating a bipolar transistor compatible with a BICMOS technology (that is, a technology enabling the simultaneous fabrication of bipolar transistors and of complementary MOS transistors) is described.--

Please replace the second paragraph on page 5, lines 4-11 with the following amended paragraph:

--Fig. 2 shows an initial step of fabrication of an NPN-type bipolar transistor according to the present invention. On an N-type epitaxial layer 101, a window is defined in a thick oxide layer 102. As an example, a layer 103 open more widely than the window ~~102~~ and which may have been used in a previous step of protection of this window during the performing of other steps has also been shown. Layer 103 is for example a silicon oxide layer of a thickness of 20 to 30 nanometers covered with a silicon nitride layer also of a thickness of 20 to 30 nanometers. This layer 103 will not be shown in the following drawings since it has no functional role in the bipolar transistor to be described.--

Please replace the fourth paragraph on page 5, lines 15-19 with the following amended paragraph:

--As an example of numeric values, in an embodiment adapted to the fabrication of submicron dimensioned integrated circuits, the thickness of thick oxide layer 102 can be around 500 nm, the thickness of P-type silicon oxide layer 105 around 200 nm, the thickness of silicon oxide layer 106 around 300 nm, and the thickness of resist layer 108 around 1000 nm (1 *m).--